ABSTRACT OF THE DISCLOSURE

A data transfer control device and method is devoted to control data transfer (i.e., DMA transfer) between a main memory whose storage capacity is arbitrarily set and a buffer memory (e.g., a FIFO memory) incorporated in a peripheral module, wherein a first register is arranged to store a first value representing a first number of times for transferring m-bit data to suit the storage capacity of the buffer memory, and a second register is arranged to store a second value representing a second number of times for transferring m-bit data to match the amount of transferring data stored in the main memory. A controller is arranged to control transferring of m-bit data based on the first value while controlling writing operations for the buffer memory. It determines the timing to output an interrupt signal to a CPU managing the main memory on the basis of the second value.